A HEMT HARMONIC OSCILLATOR STABILIZED BY AN X-BAND DIELECTRIC RESONATOR

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ABSTRACT

A simple design method for harmonic oscillators using HEMT devices is presented. The method employs non-linear analysis to derive the harmonic components of the drain current of a low frequency transistor model. The resulting harmonics components are then used to linearize a high frequency model and to synthezise the microwave circuit. The performance of a second harmonic oscillator that uses an X - Band dielectric resonator and a packaged HEMT device is +6.0 dBm output power at 18 GHz with 6.5 % RF/DC efficiency.

INTRODUCTION

The application of an active device working both as a fundamental frequency oscillator and as a frequency doubler has been succesfully applied to GUNN devices, and some of its exceptional properties has been theoretically explained[1]. The nonlinearities of two port devices has also been explored to design harmonic oscillators, and some representative reported results are as follows: 9.0 dBm at 30 GHz for a 0.5x300 μm^2 GaAs MESFET[2], 12.6 dBm at 19.6GHz for a 1.5x300 μm^2 InP MISFET[3] and 9 dBm at 18.2 GHz for a 1x400 μm^2 Dual Gate GaAs MESFET[4].

The objective of this paper is to present a simple design method for two-port harmonic oscillators, and to investigate its practical application to HEMT devices. The method relies on the device DC transfer non-linear properties to derive the drain current harmonic components of a low frequency transistor model. Then, the resulting harmonics are used in the determination of a linearized, large-signal high frequency equivalent model.

THE DESIGN APPROACH

The design of a circuit where the transistor operates both as a high level fundamental frequency oscillator and as an efficient frequency doubler, requires a compromise between the different bias point and transistor terminating impedances required for optimum performance at each function. The proposed approach to carry out this task is described next.

Non-Linear Equivalent Circuit. The HEMT is represented by the equivalent circuit of figure 1, which is similar to the one employed by MESFETs. The drain current generator is described as a function of gate and drain voltages which is capable to predict the drain current compression of HEMT devices[5]. The non-linear input capacitance is simulated by the Schottky diode capacitance equation.

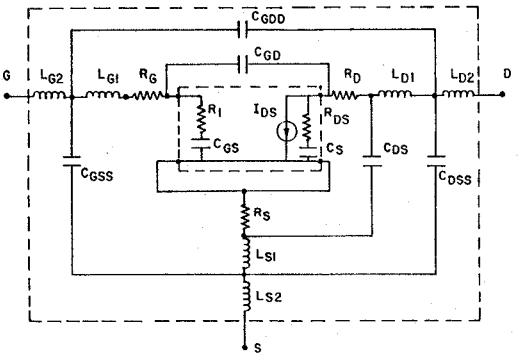

Fig. 1 Non-Linear equivalent circuit.

Low Frequency Analysis. The operation of an harmonic oscillator starts by considering the properties of a low frequency FET multiplier, where all reactive effects can be neglected. Initially, the following assumptions are made: the voltage at the input terminals is purely sinusoidal at the fundamental frequency, and the fundamental drain load is a short circuit. The gate voltage, Vg, is given by equation 1, where VGS represents the bias and Vo the amplitude of the dynamic gate voltage.

$$V_g = V_{GS} + V_o \cos(wt) \qquad (1)$$

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Applying a high dynamic voltage to the gate, the corresponding harmonic components of the current flowing into the drain, i.e., the DC component, I_{DSO}, the fundamental component, I_{DS1}, and the second harmonic component, I_{DS2}, are calculated by the equation described in reference 5. In this context, the time domain SPICE simulator was used for determining the harmonic components.

The gate bias is the first parameter to be defined and it is usually set in the vicinity of pinch-off, V_P. This is an adequate bias for a frequency multiplier concerning gain and power output, as demonstrated in previous publications[2]. But, biasing at pinch-off results in low transconductance which is not adequate for an oscillator, since the resulting loop gain may be lower than 1. Thus, in order to guarantee the start up of oscillations, the device is biased at a gate voltage greater than V_P, resulting in a reasonable value for the transconductance as shown by the bias point, Q, in figure 2.

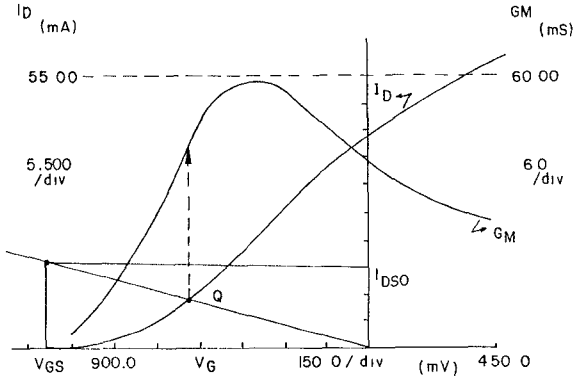

Fig. 2 DC transfer characteristics.

However, this gate bias results in lower second harmonic content on the drain current degrading the doubler efficiency. Employing a self bias approach conveys to improved operation, since the increase of the RF signal generated at the start up of oscillations conducts the gate bias to more negative values, and stabilizes at a point near the pinch-off voltage. The input DC load line that will provide this operation is obtained through the relation V_P/I_{DSO}.

In order to establish the drain bias and the conditions for optimum power performance, one must analyse the voltage and current trajectories on the input and output planes, which are shown in figure 3 for the case of a frequency doubler. The maximum drain-gate voltage that prevents avalanche of the drain-gate diode occurs when V_{DS} is maximum and the gate voltage is equal to V_{GS}. The optimum second harmonic load is determined by the relation between maximum dynamic drain voltage and maximum second harmonic drain current.

High Frequency Analysis. The first step is to linearize the transistor at the fundamental frequency by the use of the average value of the input capacitance within a RF cycle and the large signal transconductance defined by $G_m = I_{DS1}/V_O$. The harmonic oscillator topology adopted in this study is depicted in figure 4. It employs series feedback at the source terminal and a dielectric resonator coupled to the gate circuit.

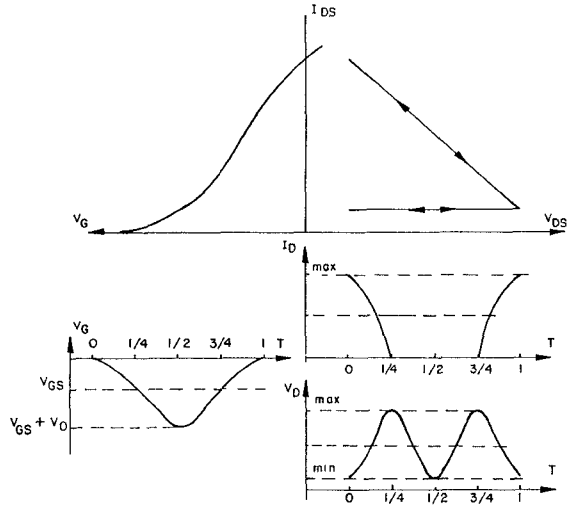

Fig. 3 Input/output waveforms.

The next step is the determination of the impedances listed in table I, at the fundamental and second harmonic frequencies. At the fundamental frequency the impedances should be purelly reactive, since any resistance will waste RF power that could be converted to the second harmonic. However, the dielectric resonator may present some associated losses, which means the gate impedance is complex.

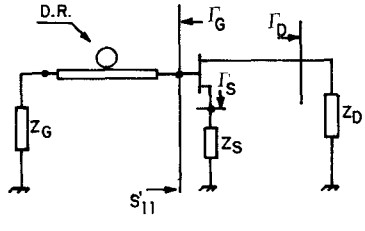

Fig. 4 Oscillator topology.

Fundamental frequency	Second harmonic
$Z_D(wo) = jX_{D1}$	$Z_D(2wo) = R_{D2} + jX_{D2}$
$Z_S(wo) = jX_{S1}$	$Z_S(2wo) = jX_{S2}$
$Z_G(wo) = R_{G1} + jX_{G1}$	$Z_G(2wo) = 50$ ohms

Table I. Impedances at the fundamental and second harmonic.

The four unknowns at the fundamental frequency were determined by varying the reflection coefficient phase presented to the drain and source, while checking the oscillating condition at the gate by equation 2 and simultaneouslly searching for a minimum voltage at the internal current source terminals. Notice at this point the difference between a multiplier and an harmonic ocillator; the drain load at the fundamental frequency is a compromise between a low impedance for high modulation of the drain current and an impedance high enough for sustaining oscillations. TOUCHSTONE linear simulator was employed to carry out this analysis.

$$\Gamma_G \cdot S_{11}' = 1 \qquad (2)$$

At the second harmonic, the gate impedance is 50 ohms, since the dielectric resonator is off resonance and the source impedance must be reactive for maximum power at the drain load. The transistor linearization is made by considering the drain current generator independant of gate voltage and equal to the second harmonic amplitude determined at low frequency. The unknowns X_{S2}, R_{D2}, and X_{D2} are determined subjected to the conditions: the second harmonic gate voltage must be minimized for minimum waste of power at the gate load; the internal drain voltage is determined by the low frequency analysis, concerning maximum power.

At this point, second harmonic feedback can be considered by calculating its voltage amplitude, V_1, at the gate. Then, the low frequency non-linear analysis is repeated using equation 3 to express the new gate voltage, where optimum phase relation has been taken into account.

$$V_g = V_{GS} + V_o \cos(wt) - V_1 \cos(2wt) \qquad (3)$$

The high frequency analysis is also repeated for the new harmonic components of the drain current. The design now reduces to the problem of determining the external circuit that presents simultaneously the impedances at the fundamental frequency and second harmonic.

TEST CIRCUIT

A packaged HEMT type NE20383A by NEC has been selected for the design, which presents a gate area of 0.3x280 μm^2. The transistor was characterized by means of DC and S-parameter techniques, and the described approach was employed to determine the terminal impedances at the fundamental and second harmonic frequencies. A dielectric resonator by THOMSON which resonates at 9 GHz and presents an unloaded "Q" of 2000 was employed in the design. The designed oscillator circuit shown in figure 5, should deliver theoretically, +7.2 dBm of second harmonic power at VDS = +2.7 Volts.

Drain Circuit. Practical realization of the circuit employing microstrip lines requires the use of a matching circuit cascaded with an harmonic filter. The desired drain reactance at the fundamental frequency is obtained by the length of line connecting the drain to the filter. The harmonic filter is composed by an association of 90^0 open stubs which blocks the fundamental frequency and the third harmonic. At the second harmonic the filter is matched to 50 ohms and the output impedance is matched by an open stub placed at a proper distance from the drain.

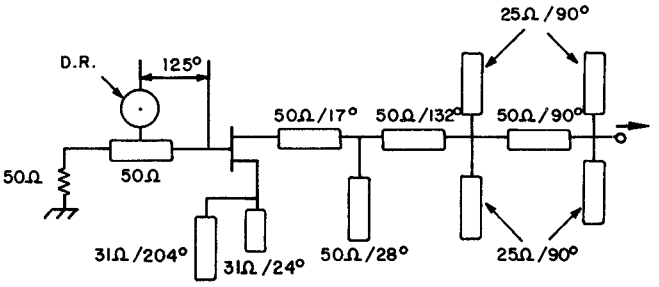

Fig. 5 Oscillator schematic circuit.

Source Circuit. Two open stubs are connected to the source, one at each lead of a double source package. It was possible to find a solution for a particular set of length and impedance line parameters that presents the desired reactances at both frequencies. The linear simulation of the circuit in a large bandwidth indicated that $S_{11}'>1$ around 4.8 GHz. In order to prevent this unwanted oscillation and simultaneouslly not disturb the design, the lentgh of one of the source stubs was increased by 180^0 at 9 GHz.

Gate Circuit. The oscillating condition at the fundamental frequency is obtained by calculating the resonator position from the gate that gives the required impedance. At the second harmonic, very low power should be wasted at the gate. However, placing an 90^0 open stub at the second harmonic, near the 50 ohm gate load, helps to adjust the second harmonic impedance, without perturbing the fundamental frequency oscillating condition and introducing negligible effects on the circuit stabilization at low frequencies.

Bias Circuitry. The bias filter is composed by two cascaded low pass structure, tuned at 9 GHz and 18 GHz respectivelly and were used to bias the drain and source. The self bias is provided by a 66 ohm placed in the source DC circuit and by the 50 ohm gate load.

The harmonic oscillator circuit was implemented on a 0.25 mm thick soft substrate, with low dielectric constant, and mounted on a metal carrier. The aluminun housing comprises two SMA connectors and a large tuning screw on the upper lid. The photograf of the oscillator is shown in figure 6.

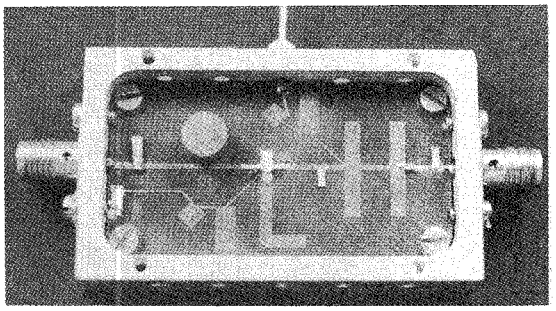

Fig. 6 Photo of the oscillator.

EXPERIMENTAL RESULTS

The resulting DC drain current with no oscillations is equal to 10 mA. After adjusting the drain stub and the dielectric resonator position to compensate the usual unpredictable parasitics and the dispersion of transistor parameters, it was observed oscillations at the specified frequency. Then, the gate stub position was adjusted for improving the output power.

The measured performance at the bias adopted in the design, VDD = +4.0 volts and IDS = 16 mA, is + 6 dBm output power at 18 GHz. The difference of 1.2 dB between the measured and predicted output power can be considered satisfactory, since the design does not take into account circuit losses, dispersion of transistor parameters, and mounting parasitics. A mechanical tuning bandwidth of 80 MHz was obtained for 1 dB output power variation. The dependance of power and efficiency on drain bias is presented in figure 7. It is noticed that power raises with drain bias, reaching a maximum of 7.2 dBm at VDD = +5 volts. This point of operation should be avoided since the transistor maximum ratings are not observed at this extreme bias.

The power at the fundamental frequency exctrated from the gate is in the order of -1.5 dBm. The rejection of the fundamental frequency at the output is -35 dBc in the worst condition within the tuning bandwidth. Another interesting feature of this circuit is its pulling characteristics: only 520 KHz frequency deviation for a VSWR of 2. This is due to the insensitivity of the fundamental mode of operation on the load variations. Frequency pushing is in the order of 250 KHz/V. The oscillator phase noise at 10 KHz from the carrier is 75 dBc/Hz.

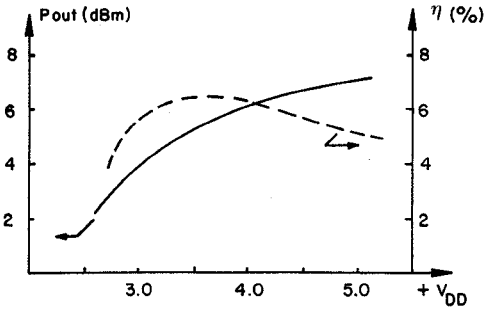

Fig. 7 Oscillator frequency and output power as a fucntion of drain bias.

CONCLUSIONS

A concise treatment on the design of harmonic oscillators has been presented. The approach of analysing the non-linear circuit at low frequencies and applying the results to high frequencies for synthesizing the connecting networks has proven to be efficient, since there is no need for extensive use of time consuming non-linear simulations at microwave frequencies. The construction of a HEMT harmonic oscillator validated the design approach, demonstrating the high performance obtained for the HEMT biased at class B.

ACKNOWLEDGMENTS

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REFERENCES

1. K. Solbach - "Simulation Study of Harmonic Oscillators". IEEE Trans. Microwave Theory Tech., MTT-30, August 1982, pp 1233-1237.
2. C. Rauscher - "High Frequency Doubler Operation of GaAs Field-Effect Transistor". IEEE Trans. Microwave Theory Tech., Vol MTT-31, June 1983, pp 462-473.
3. R. Soares, J. P. Castelletto and P. Legaud - "Performance of an InP MISFET X-Band and K-Band Oscillator-Doubler". Private Communication.
4. A. S. Chu and P. T. Chen - "An Osciplier up to K-Band Using Dual-Gate GaAs MESFET". IEEE - MTT-S International Microwave Symposium Digest, June 1980, pp 383-386.
5. F. S. Correra and E. Camargo - " 18 GHz Reverse Channel HEMT Oscillator". IEEE - MTT-S International Microwave Symposium Digest, May 1990, pp 383-386.